Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-5. (Canceled)

6. (Currently Amended) A flash memory, comprising:

a plurality of memory cells, each memory cell having a single transistor having a single control gate, a single floating gate, a single drain and a single source, said plurality of memory cells arranged in an N-row by M-column array, where N and M are integers greater than or equal to one;

N word lines, each word line connecting together the control gates of the transistors in a common and corresponding row;

M bit lines, each bit line connecting together the drains of transistors in a common and corresponding column;

wherein first and second memory cells of the plurality of memory cells are programmed by applying a first voltage to the respective control gates of the first and second memory cells, applying a second voltage to the respective sources of the first and second memory cells and grounding the respective drains of the first and second memory cells,

wherein the sources of the first and second memory cells are coupled to a common node,

wherein the sources of a plurality of memory cells are connected together to a common node,

wherein each of the sources of the memory cells includes a first doped region of a first conductivity type and a second doped region of the first conductivity type to provide a graded profile that is less abrupt than the drain.

7. (Previously Presented) The flash memory of claim 6, wherein the sources of all memory cells are connected together as a common source.

8. (Currently Amended) The flash memory of claim 6, wherein the second voltage is greater than ground potential, wherein each memory cell defines a single transistor ~~and is configured to store one bit of data~~.

9. (Currently Amended) The flash memory of claim 6, wherein the source of each memory cell is defined within ~~comprises a first doped region having a first conductivity type extending into~~ a semiconductor substrate having a second conductivity type of a charge opposite to the first conductivity type, thereby forming a first p-n junction.

10. (Currently Amended) The flash memory of claim 9, wherein the drain of each memory cell comprises a ~~second~~ third doped region of the first conductivity type, which is laterally spaced from the first doped region and extends into the substrate, thereby forming a second p-n junction.

11. (Currently Amended) The flash memory of claim ~~6~~10, wherein the first doped region comprises primarily of arsenic and the second doped region comprises primarily of phosphorous, the second doped region being provided below the first doped region, the first doped region having a doping concentration on the order of 10^{20} cm^{-3}. ~~first doped region is a double-diffused region comprising a first sub-region of a first dopant species and a second sub-region of a second dopant species, the first and second dopant species being of the first conductivity type.~~

12. (Currently Amended) The flash memory of claim 11, wherein the first doped region has a higher dopant concentration than the second doped region ~~extends deeper into the substrate than the second doped region~~.

13. (Currently Amended) The flash memory of claim 12, wherein the floating gate of each memory cell is disposed vertically above and interposed between an oxide layer and

the substrate such that the first doped region horizontally overlaps the floating gate to a greater extent than a horizontal overlap of the ~~second~~ third doped region.

14. (Currently Amended) A non-volatile device, comprising:

a substrate;

a floating gate overlying the substrate;

a control gate overlying the floating gate and being electrically coupled to a word line extending in a first direction;

a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first ~~graded~~ profile and being electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and

a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second ~~graded~~ profile ~~that is more sloped than the first graded profile~~,

wherein the first profile of the drain region has a more abrupt profile than the second profile of the source region,

wherein the control gate is applied with a first voltage of 8.5 volts or less and the source region is applied with a second voltage of 4.5 volts or less to program the non-volatile device,

wherein the floating gate, control gate, drain region, and source region together define a first memory cell ~~that is configured to store one bit of data~~,

wherein the non-volatile device further includes a second memory cell ~~that is configured to store one bit of data, the second transistor~~ including a source region that shares a common node with the source region of the first memory cell.

15. (Previously Presented) The device of claim 14, wherein the drain region is grounded to program the non-volatile device.

16. (Currently Amended) The device of claim 15, wherein the source region is a double-diffused region including first and second species of dopants.

17. (Previously Presented) The device of claim 16, wherein the first species is arsenic and the second species is phosphorous.

18. (Currently Amended) The device of claim 15, wherein an overlap between the source region and the floating gate is greater than an overlap between the drain region and the floating gate~~the first voltage is about 8.5 volts and the second voltage is about 4.5 volts~~.

19. (Currently Amended) A non-volatile semiconductor device, comprising:

a semiconductor substrate; and

a memory cell formed on the substrate, the memory cell including:

a floating gate overlying a surface of the substrate,

a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction,

a ~~first conductive~~ drain region provided in the substrate and proximate a first end of the floating gate, the ~~first conductive~~ drain region extending a first distance into the substrate and having a first ~~graded~~ profile relative to ~~the surface of~~ the substrate, the ~~first conductive~~ drain region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and

a ~~second conductive~~ source region provided in the substrate and proximate a second end of the floating gate, the ~~second conductive~~ source region being a double-diffused region that extends a second distance into the substrate and having a second ~~graded~~ profile relative to ~~the surface of~~ the substrate, the second distance being greater than the first distance~~, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile~~,

wherein the control gate is applied with a first voltage of no more than 8.5 volts and the source ~~second conductive~~ region is applied with a second voltage of no more than 4.5 volts to program the non-volatile device~~, the second voltage being a positive voltage~~,

wherein the memory cell is defined by a single transistor.

20. (Currently Amended) The device of claim 19, wherein the drain ~~first conductive region~~ is grounded to program the non-volatile device.

21. (Currently Amended) The device of claim 19, wherein the memory cell is one of a plurality of memory cells formed on the substrate, the plurality of cells being arranged in an array of N rows and M columns, each of the plurality of cells being configured to be programmed to at least a first conductive state or a second conductive state.

22. (Currently Amended) The device of claim 19, wherein source ~~the second conductive~~ region includes first and second species of dopants.

23. (Previously Presented) The device of claim 22, wherein the first species is arsenic and the second species is phosphorous.

24. (Currently Amended) The device of claim 19, wherein the first distance is ~~about~~ no more than 0.1 micron and the second distance is no more than ~~about~~ 0.3 micron.

25. (Previously Presented) The device of claim 19, wherein the second distance is about three times greater than the first distance.